**ECEN 248 - Lab Report**

**Lab Number: 1**

**Lab Title: Digital Logic Gates**

**Section Number: 519**

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**Objectives:**

The purpose of this lab is to be introduced to digital logic gates and their different behaviors. In doing so, a basic understanding of the breadboard, multimeter, and voltmeter will occur as well. These topics will be foundational in further digital circuit designs.

**Design:**

The first gate to test was the NOT gate. To test this gate we placed the NOT gate(74ALS04) with the notch up across the median of the breadboard. Connect the pins GND and VCC to the blue and red strips on the side of the breadboard, respectively. Connect the 1 NOT port in the gate(top left/1st pin) to a blue ribbon (Low) with a jumper wire. Connect the output of the 1 NOT port in the gate(2nd pin), to a multimeter with a red lead. Connect the black lead of the multimeter to the blue strip. Connect the first channel of the power supply with a piece of red information to the red ribbon and a black lead to the blue stripe on the breadboard. Turn on the multimeter and set the voltage. Turn on the power supply and set channel 1 to 5 V. Turn on channel 1. The output should be above 3 V; thus, high. Turn off channel 1. Place the input jumper wire on a red strip(High). Turn on channel 1. The output should be below 1 V. Record the two output voltages for both cases.

Repeat these steps for the AND, OR, NAND, NOR, and XOR gates use the Lab 1 note to see each gate type pin layout. Record each case and create a truth table for each logic gate.

**Results:**

| A(H/L) | Y(Volts) | Y(H/L) |
| --- | --- | --- |
| L | 4.019 | H |
| H | 0.243 | L |

**Figure 1: NOT Gate Truth Table**

| A(H/L) | B(H/L) | Y(Volts) | Y(H/L) |
| --- | --- | --- | --- |
| L | L | 0.137 | L |
| L | H | 0.137 | L |
| H | L | 0.137 | L |
| H | H | 3.912 | H |

**Figure 2: AND Gate Truth Table**

| A(H/L) | B(H/L) | Y(Volts) | Y(H/L) |
| --- | --- | --- | --- |
| L | L | 0.007 | L |
| L | H | 3.471 | H |
| H | L | 3.472 | H |
| H | H | 3.511 | H |

**Figure 3: OR Gate Truth Table**

| A(H/L) | B(H/L) | Y(Volts) | Y(H/L) |
| --- | --- | --- | --- |
| L | L | 3.427 | H |
| L | H | 3.689 | H |
| H | L | 3.591 | H |
| H | H | 0.45 | L |

**Figure 4: NAND Gate Truth Table**

| A(H/L) | B(H/L) | Y(Volts) | Y(H/L) |
| --- | --- | --- | --- |
| L | L | 3.588 | H |
| L | H | 0.751 | L |
| H | L | 0.737 | L |
| H | H | 0.712 | L |

**Figure 5: NOR Gate Truth Table**

| A(H/L) | B(H/L) | Y(Volts) | Y(H/L) |
| --- | --- | --- | --- |
| L | L | 0.01 | L |
| L | H | 3.937 | H |
| H | L | 4.419 | H |
| H | H | 0.324 | L |

**Figure 6: XOR Gate Truth Table**

**Conclusion:**

From testing the various logic gates with different Low and High input combinations, I was able to test and prove that the logic gates obey their logic functions. Also, I created simple circuits using the power supply and multimeter which will allow me to create more complex circuits in the future.

**Post-lab Deliverables:**

The truth tables above and the data sheet are attached to the submission.